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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/780,140	02/17/2004	William E. Dougherty JR.	YOR920030437US1 (8728-653	9678

46069 7590 08/06/2007

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EXAMINER	
DINH, PAUL	

ART UNIT	PAPER NUMBER
2825	

MAIL DATE	DELIVERY MODE
08/06/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/780,140	DOUGHERTY ET AL.	
	Examiner	Art Unit	
	Paul Dinh	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 June 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This is a response to the RCE and amendment filed on filed on 6/15/07.

Claims 1-20 are pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form The basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) The invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claim 14 and similarly recited claims 1 and 13 are rejected under 35 U.S.C. 102(e) as being anticipated by the prior art of record Scheffer (USP 6543041)

Means for creating a structural metric from a logic network during a logical synthesis stage (fig 1) of a circuit design model, wherein the is derived from a RTL textual description (fig 1) of the circuit design model, and the structural metric is a measure of wiring congestion (col 3 lines 62-64, fig 1, 3) of the circuit design model after physical design; and

Means for using the structural metric during the logic synthesis stage (fig 1) to predict wiring congestion of the circuit design model after the physical design to optimize the circuit design model (col 3 lines 62-64, fig 1, 3)

2. Claim 14 and similarly recited claims 1 and 13 are rejected under 35 U.S.C. 102(e) as being anticipated by the prior art of record Weaver (US pub. 2004/0230933)

Means for creating a structural metric from a logic network during a logical synthesis stage (block 2 in the figure (only one figure)) of a circuit design model, wherein the is derived from a RTL textual description (par 0015) of the circuit design model, and the structural metric is a measure of wiring congestion (block 8) of the circuit design model after physical design; and

Means for using the structural metric during the logic synthesis stage (block 2) to predict wiring congestion (block 8) of the circuit design model after the physical design (see placement/routing/layout in the figure) to optimize the circuit design model.

3. Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by the prior art of record McElvain (US pub 2006/0095872)

(Claim 14 and similarly recited claims 1 and 13)

Means for creating a structural metric from a logic network during a logical synthesis stage (fig 22, 35) of a circuit design model, wherein the is derived from a RTL textual description (fig 22, 35) of the circuit design model, and the structural metric is a measure of wiring congestion of the circuit design model after physical design (fig 23, 35, par 0111, 0126); and

Means for using the structural metric during the logic synthesis stage (fig 22, 35) to predict wiring congestion of the circuit design model after the physical design (fig 23, 35, par 0111, 0126) to optimize the circuit design model.

(Claim 2) wherein using the structural metric to optimize circuit design model comprises adding, deleting or substituting one or more circuits using a combination of Boolean, algebraic and electrical optimizations (fig 22, 26, 35, 43-44).

(Claims 3, 15) wherein the structural metric includes a measure of routing congestion of the circuit design model after placement and routing design (fig 23, 35, par 0111, 0126), the routing congestion being measured by an average and a peak number of wires crossing any bisection of the placed and routed circuit design model (i.e., fig 15, 37-41, par 0109, 0111, 0126)

(Claims 4-5) wherein using the structural metric to optimize the circuit design model comprises using the structural metric: during a technology independent synthesis stage of the logic synthesis stage (fig 22, 35); during the technology mapping stage of the logic synthesis (fig 22, 35).

(Claim 6) wherein using the structural metric during the logic synthesis stage to optimize the circuit design comprises using the structural metric during a buffering stage of the logic synthesis stage (fig 26, par 0011, 0122)

(Claims 7-9, 16-18) further comprising incrementally updating the structural metric when logic changes are made to the circuit design model comprises: performing recomputation on circuits involved in an optimization and circuits affected by the optimization to provide a structural metric cost (fig 22, 43-44); maintaining information regarding circuits affected by an optimization, which are computed when recomputation of the structural metric is necessary (fig 22, 43-44).

(Claims 10, 19) wherein creating the structural metric comprises **any one of** a distance metric, a sum-of-all-pairs-min-cut ("SAPMC"), expansion metric (any one of fig 26, 28-29)

(Claims 11, 20) wherein determining a structural metric comprises: generating **one or more** possible optimizations (this invention about generating one or more possible optimizations i.e., cost, components, power, area, delay, reduction/minimizing manual work, cut, net, congestion, hardware, distance, wire lengths, etc.); incrementally updating the structural metric when the optimizations are made to the circuit design to evaluate the cost of applying each of the **one or more** possible optimizations to the circuit design necessary (fig 22, 43-44), the structural metric comprising ***any one of*** a distance metric, a sum-of-all-pairs-min-cut ("SAPMC"), and an expansion metric (any one of fig 26, 28-29); evaluating a structural metric cost of each of the **one or more** possible optimizations as given by the structural metric (fig 22, 43-44); selecting an optimization from the *one or more* possible optimizations with the lowest structural metric cost (par 0013, 0104); and applying the optimization to the circuit (fig 22, 43-44)

(Claim 12) wherein generating the **one or more** possible optimizations comprises: generating a structure-driven kernel factoring; generating a structure-driven decomposition; generating a structure-driven tech mapping; and generating a structure-aware buffering (i.e., fig 26, par 0005, 0123).

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Dinh whose telephone number is 571-272-1890. If attempts to reach the examiner by telephone are unsuccessful, the examiner's Supervisor, Jack Chiang can

be reached on 571-272-7483. The fax number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Paul Dinh
Primary Examiner